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26794

7590

11/21/2008

TYCO TECHNOLOGY RESOURCES  
4550 NEW LINDEN HILL ROAD, SUITE 140  
WILMINGTON, DE 19808-2952

EXAMINER

GUZMAN, APRIL S

ART UNIT

PAPER NUMBER

2618

DATE MAILED: 11/21/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,375	12/16/2003	Mark F. Kelcourse	17988A (1521-R-CP-02)	5358

TITLE OF INVENTION: APPARATUS, METHODS AND ARTICLES OF MANUFACTURE FOR A MULTI-BAND SWITCH

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	02/23/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS** FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

## HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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26794 7590 11/21/2008  
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**WILMINGTON, DE 19808-2952**

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,375	12/16/2003	Mark F. Kelcourse	17988A (1521-R-CTP-02)	5358

**TITLE OF INVENTION: APPARATUS, METHODS AND ARTICLES OF MANUFACTURE FOR A MULTI-BAND SWITCH**

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	02/23/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
GUZMAN, APRIL S	2618	455-078000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.  
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 \_\_\_\_\_  
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 \_\_\_\_\_  
3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

**PLEASE NOTE:** Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee  
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☐ Advance Order - # of Copies \_\_\_\_\_

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☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Typed or printed name \_\_\_\_\_ Registration No. \_\_\_\_\_

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,375	12/16/2003	Mark F. Kelcourse	17988A (1521-R-CIP-02)	5358
26794	7590	11/21/2008	EXAMINER	
GUZMAN, APRIL S				
ART UNIT			PAPER NUMBER	

2618

DATE MAILED: 11/21/2008

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 1374 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 1374 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

# Notice of Allowability

## Application No.

10/737,375

## Examiner

APRIL S. GUZMAN

## Applicant(s)

KELCOURSE ET AL.

## Art Unit

2618

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 08/14/2007.
2. ☒ The allowed claim(s) is/are 1-3,9-13,21-23 and 25-30.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some\* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

## Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date 11/04/04, 06/17/08
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_.

## DETAILED ACTION

### *Response to Amendment*

The Examiner acknowledges the receipt of the Applicant's amendment filed on 08/14/2007. Claims 4-8, 14-20 and 24 have been canceled. Claims 1, 9-13, 21-23 have been amended. Claims 25-30 have been added. **Claims 1-3, 9-13, 21-23, and 25-30** are therefore currently pending in the present application.

### *Allowable Subject Matter*

**Claims 1-3, 9-13, 21-23, and 25-30** are allowed.

Consider **claim 1**, the best prior art of record found during the examination of the present application, Gerlach (U.S. Patent # 6,518,855) in view of Khabbaz (U.S. Patent # 6,351,183), fail to specifically teach, suggest or disclose a single-die integrated circuit for switching among a plurality of transmission ports and a plurality of received reports, comprising: a transmitter switching section having a plurality of transmission ports, said transmitter switching section operable to switch a selected one of the plurality of transmission ports to a transmission node wherein, *for each transmission port, the transmission switching section includes a plurality of FETs having current paths coupled in series with each other* and operable to couple the transmission port to the transmission node, wherein *a first one of the FETs proximate the respective transmission port has a current path with a first end coupled to the transmission port and a gate; a first feed-forward capacitor coupled between said first end of said current path and said gate of said first one of the FETs*; and a receiver switching section having a plurality of received ports, said receiver switching section operable to switch a selected one of the plurality of received reports to the transmission node.

Gerlach teach semiconductor switching elements such as field effect transistors which are integrated on a circuit in the form of a Monolithic Microwave Circuit. The circuit is connected to at least two transmitting apparatuses and at least two receiving apparatuses in which case the transmitters and receivers respectively differ in that they operate on different frequency bands (column 1 lines 41-67 and column 2 lines 20-54). Gerlach also teach a first transmitter which is used for frequency band 1, is connected to antenna 1, the receiver for frequency band 2 is connected to antenna 2. The circuit is constructed monolithically in an integrated manner. The switch 1 is formed by FETS 9 to 12. FETs 9 and 11 as well as 10 and 12, respectively, are working together to connect Tx Band 1 or TX Band 2 with terminal Tx. FETs 9 and 12 are controlled by varying the gate potential, FETs 11 and 10 are controlled by varying the potentials of the source of the drain (column 3 lines 18-62).

Khabbaz teach a switched amplifying device according to an embodiment of the present invention designed to amplify over a 1.8 GHz to 2 GHz frequency band and having two gain stages in a cascade configuration. The dual gain stage embodiment of the switched amplifying device comprises the amplifying FET (8), which in the dual gain stage embodiment is termed a first amplifying FET (8), and a second amplifying FET (108). The first amplifying FET (8) produces an amplified signal at the drain (9). The switched amplifying device further comprises a second amplifying FET having a gate (111) which is coupled to receive and further amplify the amplified signal to achieve higher gain than in the single gain stage embodiment shown in FIG. 4 of the drawings. The drain (9) of the first amplifying FET (8) is connected to the gate (111) of the second amplifying FET (108) through a matching series capacitor (50) (Figure 8, column 6 lines 55-67 and column 7 lines 1-40).

These teachings clearly differ from the present application, therefore, claim 1 is considered novel and non-obvious over the prior art and therefore is allowed.

Claims 2-3, 9, and 25-27 depend on allowable claim 1, therefore these claims are also allowed.

Consider **claim 10**, the best prior art of record found during the examination of the present application, Gerlach (U.S. Patent # 6,518,855) in view of Khabbaz (U.S. Patent # 6,351,183), fail to specifically teach, suggest or disclose a single-die multiband switch for wireless communication, comprising: an antenna port; a plurality of transmitter ports, for each transmitter port a switching topology operable to switch the transmitter port to the antenna port; and a plurality of received ports, a switching topology operable to switch a selected one of said receiver ports to the antenna port, said switching topologies comprising a multiple-stage switching circuit, *a first stage of the multiple-stage switching circuit selectively connecting or isolating the antenna port from the multiple-stage switching topology, and a last stage of the multiple-stage switching topology selectively connecting or isolating a plurality of the receiver ports from the multi-stage switching topology*, wherein said last stage includes, for each receiver port, *a signal path FET having a current path controllable to connect the receiver port to an intermediate node*, said first stage operable to connect the intermediate node to the antenna port, and *wherein each said signal path FET has a gate to which a control signal is applied, a shunt FET having a drain coupled to the gate of the signal path FET, a source coupled to ground, and operable to enhance isolation of the receiver port from the intermediate node when the signal path FET is in and OFF state.*

Gerlach teach semiconductor switching elements such as field effect transistors which are integrated on a circuit in the form of a Monolithic Microwave Circuit. The circuit is connected to at least two transmitting apparatuses and at least two receiving apparatuses in which case the transmitters and receivers respectively differ in that they operate on different frequency bands (column 1 lines 41-67 and column 2 lines 20-54). Gerlach also teach a first transmitter which is used for frequency band 1, is connected to antenna 1, the receiver for frequency band 2 is connected to antenna 2. The circuit is constructed monolithically in an integrated manner. The switch 1 is formed by FETS 9 to 12. FETs 9 and 11 as well as 10 and 12, respectively, are working together to connect Tx Band 1 or TX Band 2 with terminal Tx. FETs 9 and 12 are controlled by varying the gate potential, FETs 11 and 10 are controlled by varying the potentials of the source of the drain (column 3 lines 18-62).

Khabbaz teach a switched amplifying device according to an embodiment of the present invention designed to amplify over a 1.8 GHz to 2 GHz frequency band and having two gain stages in a cascade configuration. The dual gain stage embodiment of the switched amplifying device comprises the amplifying FET (8), which in the dual gain stage embodiment is termed a first amplifying FET (8), and a second amplifying FET (108). The first amplifying FET (8) produces an amplified signal at the drain (9). The switched amplifying device further comprises a second amplifying FET having a gate (111) which is coupled to receive and further amplify the amplified signal to achieve higher gain than in the single gain stage embodiment shown in FIG. 4 of the drawings. The drain (9) of the first amplifying FET (8) is connected to the gate (111) of the second amplifying FET (108) through a matching series capacitor (50) (Figure 8, column 6 lines 55-67 and column 7 lines 1-40).



These teachings clearly differ from the present application, therefore, claim 10 is considered novel and non-obvious over the prior art and therefore is allowed.

Claims 11-13 depend on allowable claim 10, therefore these claims are also allowed.

Consider **claim 21**, the best prior art of record found during the examination of the present application, Gerlach (U.S. Patent # 6,518,855) in view of Khabbaz (U.S. Patent # 6,351,183), fail to specifically teach, suggest or disclose a method of switching one of a plurality of transmitters and a plurality of receivers to a transmitter/receiver antenna, comprising the steps of: connecting each transmitter to a respective one of the plurality of transmitter ports formed on a single integrated circuit die; connecting each receiver to a respective one of a plurality of received reports formed on the die; controlling a selected one of a plurality of switching topologies~ each associated with a respective one of the transmitter and receiver ports~ to connect a respective selected one of the transmitter and receiver ports to an antenna port formed on the die; and controlling other ones of the switching topologies to isolate others of the transmitter and receiver ports from the antenna port; *for a selected one of the receiver or transmitter ports, switching a transistor having a signal path between an associated one of the receiver or transmitter ports and the antenna to an ON state to pass a signal from said associated receiver or transmitter port through said current path of the signal path transistor; turning off an associated shunt transistor having a drain connected to a gate of the at least one signal path transistor so as to isolate the gate from ground; for at least one other receiver or transmitter port, switching a transistor having a signal path between an associated one of the receiver or transmitter ports and the antenna to an OFF state; and turning on an associated shunt transistor having a drain connected to a gate of the at least one other signal path*

*transistor such that the gate is coupled to ground so as to enhance the isolation of the at least one other receiver or transmitter port from the associated receiver or transmitter port.*

Therefore, claim 21 is considered novel and non-obvious over Gerlach in view of Khabbaz, therefore claim 21 is allowed.

Claims 22-23 depend on allowable claim 21, therefore claims 22-23 are also allowed.

Consider **claim 28**, the best prior art of record found during the examination of the present application, Gerlach (U.S. Patent # 6,518,855) in view of Khabbaz (U.S. Patent # 6,351,183), fail to specifically teach, suggest or disclose a single-die integrated circuit for switching among a plurality of transmission ports and a plurality of received reports, comprising: a transmitter switching section having a plurality of transmission ports, said transmitter switching section operable to switch a selected one of the plurality of transmission ports to a transmission node wherein, for each transmission port, *the transmission switching section includes a plurality of FETs having current paths coupled in series with each other and operable to couple the transmission port to the transmission node, wherein a last one of the FETs proximate the transmission node has a current path with a first end coupled to the transmission node and a gate; a first feed-forward capacitor coupled between said first end of said current path and said gate of said last one of the FETs*; and a receiver switching section having a plurality of received ports, said receiver control section operable to switch a selected one of the plurality of received reports to the transmission node.

Gerlach teach semiconductor switching elements such as field effect transistors which are integrated on a circuit in the form of a Monolithic Microwave Circuit. The circuit is connected to at least two transmitting apparatuses and at least two receiving apparatuses in which case the

transmitters and receivers respectively differ in that they operate on different frequency bands (column 1 lines 41-67 and column 2 lines 20-54). Gerlach also teach a first transmitter which is used for frequency band 1, is connected to antenna 1, the receiver for frequency band 2 is connected to antenna 2. The circuit is constructed monolithically in an integrated manner. The switch 1 is formed by FETS 9 to 12. FETs 9 and 11 as well as 10 and 12, respectively, are working together to connect Tx Band 1 or TX Band 2 with terminal Tx. FETs 9 and 12 are controlled by varying the gate potential, FETs 11 and 10 are controlled by varying the potentials of the source of the drain (column 3 lines 18-62).

Khabbaz teach a switched amplifying device according to an embodiment of the present invention designed to amplify over a 1.8 GHz to 2 GHz frequency band and having two gain stages in a cascade configuration. The dual gain stage embodiment of the switched amplifying device comprises the amplifying FET (8), which in the dual gain stage embodiment is termed a first amplifying FET (8), and a second amplifying FET (108). The first amplifying FET (8) produces an amplified signal at the drain (9). The switched amplifying device further comprises a second amplifying FET having a gate (111) which is coupled to receive and further amplify the amplified signal to achieve higher gain than in the single gain stage embodiment shown in FIG. 4 of the drawings. The drain (9) of the first amplifying FET (8) is connected to the gate (111) of the second amplifying FET (108) through a matching series capacitor (50) (Figure 8, column 6 lines 55-67 and column 7 lines 1-40).

These teachings clearly differ from the present application, therefore, claim 28 is considered novel and non-obvious over the prior art and therefore is allowed.

Claim 29 depend on allowable claim 28; therefore claim 29 is also allowed.

Consider **claim 30**, the best prior art of record found during the examination of the present application, Gerlach (U.S. Patent # 6,518,855) in view of Khabbaz (U.S. Patent # 6,351,183), fail to specifically teach, suggest or disclose a single-die integrated circuit for switching among a plurality of transmission ports and a plurality of received reports, comprising: a transmitter switching section having a plurality of transmission ports, said transmitter switching section operable to switch a selected one of the plurality of transmission ports to a transmission node wherein, for each transmission port, *the transmission switching section includes a plurality of FETs having current paths coupled in series with each other and operable to couple the transmission port to the transmission node; a bypass resistor coupled in parallel with the current paths of the plurality of FETs in series*; and a receiver switching section having a plurality of received ports, said receiver switching section operable to switch a selected one of the plurality of received reports to the transmission node.

Gerlach teach semiconductor switching elements such as field effect transistors which are integrated on a circuit in the form of a Monolithic Microwave Circuit. The circuit is connected to at least two transmitting apparatuses and at least two receiving apparatuses in which case the transmitters and receivers respectively differ in that they operate on different frequency bands (column 1 lines 41-67 and column 2 lines 20-54). Gerlach also teach a first transmitter which is used for frequency band 1, is connected to antenna 1, the receiver for frequency band 2 is connected to antenna 2. The circuit is constructed monolithically in an integrated manner. The switch 1 is formed by FETS 9 to 12. FETs 9 and 11 as well as 10 and 12, respectively, are working together to connect Tx Band 1 or TX Band 2 with terminal Tx. FETs 9 and 12 are

controlled by varying the gate potential, FETs 11 and 10 are controlled by varying the potentials of the source of the drain (column 3 lines 18-62).

Khabbaz teach a switched amplifying device according to an embodiment of the present invention designed to amplify over a 1.8 GHz to 2 GHz frequency band and having two gain stages in a cascade configuration. The dual gain stage embodiment of the switched amplifying device comprises the amplifying FET (8), which in the dual gain stage embodiment is termed a first amplifying FET (8), and a second amplifying FET (108). The first amplifying FET (8) produces an amplified signal at the drain (9). The switched amplifying device further comprises a second amplifying FET having a gate (111) which is coupled to receive and further amplify the amplified signal to achieve higher gain than in the single gain stage embodiment shown in FIG. 4 of the drawings. The drain (9) of the first amplifying FET (8) is connected to the gate (111) of the second amplifying FET (108) through a matching series capacitor (50) (Figure 8, column 6 lines 55-67 and column 7 lines 1-40).

These teachings clearly differ from the present application, therefore, claim 30 is considered novel and non-obvious over the prior art and therefore is allowed.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: see PTO-892 Notice of References Cited.

Any response to this Office Action should be **faxed to (571) 273-8300 or mailed to:**

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401 Dulany Street  
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to April S. Guzman whose telephone number is 571-270-1101. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Anderson can be reached on 571-272-4177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/April S. Guzman/  
Examiner, Art Unit 2618

/Matthew D. Anderson/  
Supervisory Patent Examiner, Art Unit 2618